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(54) **SYSTEM FOR CODING AND DECODING BINARY DATA.**

(57) A binary data coding system particularly adapted for a magnetic recording and reproduction, which system limits the minimum and maximum values of a reverse magnetization distance so as to obtain a higher recording density. Binary data are divided by every 2 bits and the code of every 2 bits is input into a read-only memory (7) together with the adjacent codes before and behind, e.g., the preceding 2 bits and the following 4 bits and then output after converted into a 4-bit code. In the bit arrangement of the converted code, the number of the code bits "0" present sequentially between the code bit "1" at an arbitrary point and the following code bit "1" is limited, for example, in a range of 2 to 8. The converted code-signal line is magnetically recorded in such a manner that a reverse magnetization is made corresponding to every code bit "1".

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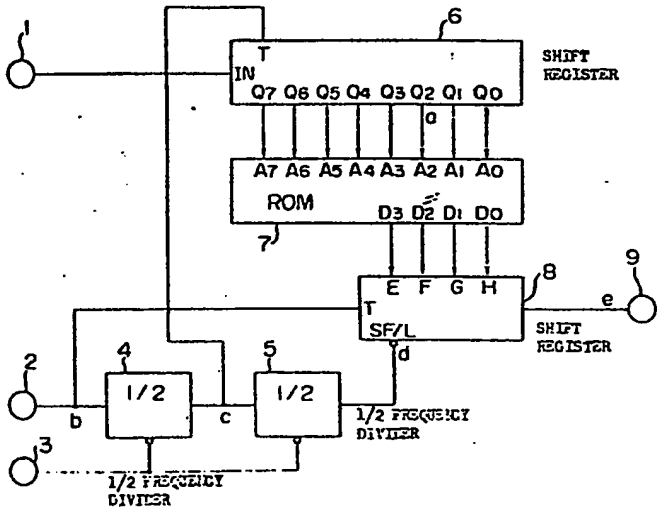

1
6
T
IN
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
SHIFT REGISTER
a
A7 A6 A5 A4 A3 A2 A1 A0
ROM
D3 D2 D1 D0
7
9
8
E F G H
T
SF/L
e
SHIFT REGISTER
d
2
4
5
1/2
1/2
b
c
1/2 FREQUENCY DIVIDER
3
1/2 FREQUENCY DIVIDER

SPECIFICATION
ENCODING AND DECODING SYSTEMS FOR BINARY DATA

TECHNICAL FIELD

This invention relates to a binary data encoding system for converting a sequence of binary data to a sequence of binary codes suitable for the recording upon recording the original binary data on a record medium such as a magnetic tape or a magnetic disc, and a decoding system for decoding and converting the sequence of converted binary codes upon reproducing it from the record medium.

BACKGROUND ART

In order to increase a recording density upon recording binary data on a record medium such as a magnetic tape or a magnetic disc there are previously proposed and practiced various encoding systems.

Fig. 1 is an explanatory diagram of one example of a conventional encoding system and Fig. 1(a) shows one example of a bit pattern of an original binary data sequence wherein numerals 0 and 1 express logic "0" and "1" respectively and T_o indicates a bit interval. The same Figs. (b) and (d) are one example of conventional encoding systems, the same Fig. (b) is called an MFM system (modified FM system) and the same Fig. (d) is called a 3 PM system (3 position modulation system. As examples of sorts of appliances applied to the respective systems, the MFM system is used with magnetic disc devices (3330, 3340, 3350 etc.) of IBM firm and the 3 PM system is used with a magnetic disc device

encoding system a sequence of m-bit binary data is converted to a sequence of n-bit binary codes ($n \geq m$) and between a code bit "1" selected at will from the code sequence after the conversion and a code bit "1" next developed there exist code bits "0" whose number has a minimum of d and a maximum of k, the following expressions (1) to (4) hold:

$$T_{min}\begin{pmatrix}\text{spacing between}\\ \text{inversions of minimum}\\ \text{magnetization}\end{pmatrix} = \frac{m}{n}(d+1)T_0 \qquad (1)$$

$$T_{max}\begin{pmatrix}\text{spacing between}\\ \text{inversions of maximum}\\ \text{magnetization}\end{pmatrix} = \frac{m}{n}(k+1)T_0 \qquad (2)$$

$$C_{LK}\begin{pmatrix}\text{period of demodulating}\\ \text{clock signal}\end{pmatrix} = \frac{m}{n}T_0 \qquad (3)$$

and

$$T_W\begin{pmatrix}\text{demodulation}\\ \text{phase margin}\end{pmatrix} = \frac{m}{n}T_0 \qquad (4)$$

where T_0 is a period of original data.

Accordingly from the foregoing description values of the expressions (1) and (2) are preferably larger (the abovementioned items (a) and (b)) and also the undermentioned ratio of the spacing between the inversions of maximum magnetization to the period of the demodulating clock signal (the expression (5)) and the undermentioned ratio of the spacing between the inversions of maximum magnetization to that between the inversions of minimum magnetization (the expression (6)) are preferably smaller (the abovementioned items (c) and (d)).

$$\frac{T_{max}}{C_{LK}} = \frac{m}{n}(k+1)T_0 \Big/ \frac{m}{n}T_0 = k+1 \qquad (5)$$

$$\frac{T_{max}}{T_{min}} = \frac{m}{n}(k+1)T_0 \Big/ \frac{m}{n}(d+1)T_0 = \frac{k+1}{d+1} \qquad (6)$$

With respect to the MFM system, the 3 PM system and the encoding system according to the present invention, the foregoing parameters are shown in the following Second Table:

2ND TABLE

Table of Comparison of Parameters in Respective Encoding Systems

Parameter / Mod. System	Spa. btwn. Invs. of Min. Magzn.	Demodg. Phase Marg.	Spa. btwn. Invs. of Max. Magzn./ Period of Demodg. Clock Sig.	Spa. btwn. Invs. of Max. Magzn./ Spa. btwn. Invs. of Min. Magzn.
MFM System	$0.5T_0$	$0.5T_0$	4	2
3 PM System	$1.5T_0$	$0.5T_0$	12	4
System of This Invention	$1.5T_0$	$0.5T_0$	9	3

DISCLOSURE OF THE INVENTION

An encoding system according to the present invention, upon dividing a binary data sequence at intevals of two bits and converting those divided 2-bit data to codes each consisting of four bits, senses data within six bits preceding and continuous to said 2-bit data and also within succeeding six bits succeeding thereto, utilizes said data thus sensed

to convert said 2-bit data to said 4-bit codes and causes not smaller than two to not larger than eight of code bits "0" to exist between any code bit "1" in a sequence of those converted codes and a code bit "0" next developed therein. Thereby it has the properties that, as shown in the Second Table, it is excellent over the MFM system in spacing between the inversions of minimum magnetization and over the 3 PM system in ability to produce the demodulating clock signal from a reproduced signal (the spacing between the inversions of maximum magnetization/ the period of the demodulating clock signal) and in ability of reproduced waveforms to interfere with one another (the spacing between the insersions of maximum magnetization/ the spacing between inversions of minimum magnetization). Also it can decrease the occurrence of errors during the decoding.

$d/k = 2/8$

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is explanatory diagrams of conventional encoding systems of the MFM and 3 PM systems; Fig. 2 is a block diagram of one embodiment to which an encoding system according to the present invention is applied; Fig. 3 is a block diagram of another embodiment to which another encoding system according to the present invention is applied; Fig. 4 is a timing chart for explaining the operation of the embodiments shown in Figs. 2 and 3; Fig. 5 is a block diagram of one embodiment to which a decoding system according to the present invention is applied; and Fig. 6 is a timing chart for explaining the operation of the embodiment shown in Fig. 6.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention will hereinafter described in detail in conjunction with embodiments shown in the accompanying drawings. The undermentioned Third and Fourth Tables are one concrete example of a conversion algorithm of a novel encoding system. The conversion algorithm is to divide first original data at intervals of two bits and convert those divided 2-bit data to 4-bit codes following the rule of the Third or Fourth Table. By observing code sequences converted in accordance with the foregoing conversion algorithm, $T_W = 0.5T_0$ results because the parameters hold m/n = 2/4 = 0.5.

3RD TABLE

Table (1) of Conversion Algorithm of Novel Encoding System

Original Data	Converted Code	Conditions
11	Y000	
01	0010	
10	0100	"E_2E_1" ≠ "10" and "L_1L_2" = "00"
10	0001	"E_2E_1" = "10" and "L_1L_2" = "00"
10	0000	"E_2E_1" = "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	0100	"E_2E_1" ≠ "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	Y001	Except the Foregoing
00	0000	"E_2E_1" = "10"
00	0100	Except the Foregoing

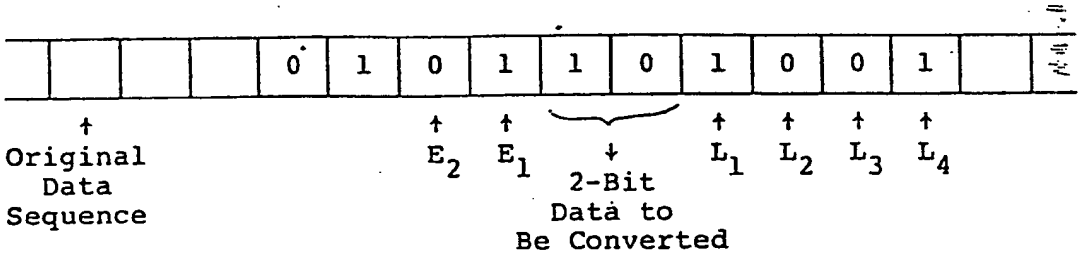
where E_n : data bits preceding by n-bits, 2-bit data to be converted in original data sequence

L_n : data bits succeeding by n-bits, 2-bit data to be converted in original data sequence

and

Y : complement logic of logical sum of two bits immediately before code bit Y in converted code sequence supplimentation

A : Explanation of E_1 to E_2 and L_1 to L_2



B : Explanation of Y

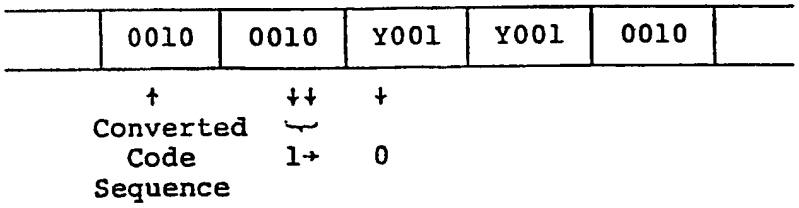


Table (2) of Conversion Algorithm of Novel Encoding System

Original Data	Converted Code	Conditions
11	Y000	
01	0010	
10	0100	"E_2E_1" ≠ "10" and "L_1L_2" = "00"
10	0001	"E_2E_1" = "10" and "L_1L_2" = "00"
10	0000	"E_2E_1" = "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	0100	"E_2E_1" ≠ "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	Y001	Except the Foregoing
00	0000	"E_2E_1" = "10" and "E_4E_3" ≠ "10"
00	0010	"E_2E_1" = "10" and "E_4E_3" = "10"
00	0100	Except the Foregoing

Also in the case the Third Table is used as patterns when the conversion gives d and k, original data

··· 01 00 11 ··· results in converted codes

·· "0010" "0100" "1000" ·· and d=2 holds. Also original data

··· 01 10 00 01 ··· results in vonverted codes

·· "0010" "0100" "0000" "0010" ·· and k = 8 holds. In this way d = 2 and k = 8 are given and it will be understood that the Second Table is fulfilled as the abilities of the parameters.

Subsequently regarding the conversion algorithm shown in the Third Table the ruling property of its conversion is considered. Further the Fourth Table is of a conversion into which the Third Table is partly rivised and concretely identical to the Third Table.

The ruling properly is to divide original data at intervals of two bits and convert them in accordance with the fundamental conversion table of a Fifth Table.

5TH TABLE

Fundamental Conversion Table of Novel Encoding System

Original Data	Converted Code
11	Y000
01	0010
10	Y001
00	0100

Y = complement logic of logical sum of two bits immediately before code bit Y in converted code sequence

Y	Two Bits Immediately before Code Bit Y
1	"00"
0	Except for "00"

From the fundamental conversion table of the Fifth Table it is understood that not more than d = 2 and k = 8 are satisfied in the conversion unless "10" and "00" express two consecutive patterns each including two bits in the original data to be converted. Therefore upon the occurrence of the patterns "10" and "00", the conversion of all the patterns is arranged to satisfy d = 2 and k = 8 by changing the fundamental conversion table of the Fifth Table to the revised conversion method as shown in the Third and Fourth Tables.

Fig. 2 is a block diagram of one embodiment to which an encoding system according to the present invention is applied and Fig. 4 is a timing chart for explaining its operation. In Fig. 2 the original data are entered into a shift register (6) through an input terminal (1). Also an input terminal 2 has entered thereinto a clock signal b (Fig. 4(b)) which signal doubles a clock signal for the original data and further the clock signal b is frequency divided into a signal c with a frequency divided by 2 (Fig. 4(c)) and a signal d with a frequency divided by 4 (Fig. 4(d)) by 1/2 frequency dividers (4) and (5) respectively. In a shift resistor (serial in-paralle out) (6) the entered original data are delayed one bit at a time with the clock signal c applied to a terminal (T) and delivered through data output terminals (Q_7 to Q_0). A signal a delivered at that time through the output terminal (Q_2) is shown in Fig. 4(a). Data outputs (Q_7 to Q_0) are entered into input terminals (A_7 to A_0) to an ROM (a read only memory, for example, SN74S471N of TI firm or the like)

having an algorithm shown in the undermentioned Sixth Table and a code converted output signal is provided through its output terminals D_3 to D_0).

6TH RABLE

Table (1) of Algorithm of Converting ROM of Novel Encoding System

Input Address								Output Pattern			
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_0	D_1	D_2	D_3
1	1	1	1					1	0	0	0
0	0	1	1					1	0	0	0
		0	1					0	0	1	0
0	0	1	0	0	0			0	1	0	0
0	1	1	0	0	0			0	1	0	0
1	1	1	0	0	0			0	1	0	0
0	0	1	0	1	0	0	0	0	1	0	0
0	1	1	0	1	0	0	0	0	1	0	0
1	1	1	0	1	0	0	0	0	1	0	0
1	1	1	0	Z				1	0	0	1
0	0	1	0	Z				1	0	0	1
0	1	1	0	Z				0	0	0	1
1	0	1	0	R				0	0	0	1
0	0	0	0					0	1	0	0
0	1	0	0					0	1	0	0
1	1	0	0					0	1	0	0
Addresses Except for the Foregoing								0	0	0	0

where Z : All addresses A_4 to A_7 satisfying

"A_4A_5" $\neq$ "00" and "$A_4A_5A_6A_7$" $\neq$ "1000"

R : All addresses A_4 to A_7 satisfying

"$A_4A_5A_6A_7$" $\neq$ "1000"

and portions with the diagonal have no address appointed thereto and therefore have any values

This 4-bit output is entered into a shift register (parallel in-serial out)(8) at the resetting terminals (H to E). More specifically, a presetting signal is latched with a synchronized timing signal d (Fig. 4d) applied to a terminal (SF/ℓ) for each of 2-bit data to be converted and converted 4-bit codes are delivered, as a serial output signal e (Fig. 4e), to an output terminal (9) by means of the clock signal b (Fig. 4b) applied to the terminal (T). Further because of the necessity of causing the right synchronization of two bits of the data to be converted, the 1/2 frequency dividers (4) and (5) are set in polarity with a synchronization sensing signal (which is entered into an input terminal (3)) such as a data synchrnozining signal inserted into the original data sequence for each of predetermined bit lengths.

It will be understood that the pattern (11010001) of the original data shown in Fig. 4(a) is converted to a code pattern (1000001001000010) through that operation.

The undermentioned Seventh and Eighth Tables are other concrete examples of the conversion algorithm of the

novel encoding system. As in the Third and Fourth Tables as described above, the original data are first divided at intervals of two bits and those divided 2-bit data are converted to 4-bit codes following the rule of the Seventh or Eighth Table. By observing a code sequence converted in accordance with the foregoing conversion algorithm, $T_W = 0.5T_0$ results because the parameters hold m/n = 2/4 = 0.5.

7TH TABLE

Table (3) of Conversion Algorithm of Novel Encoding System

Original Data	Converted Code	Conditions
11	Y000	
01	0010	
10	0100	"E_2E_1" ≠ "10" and "L_1L_2" = "00"
10	0001	"E_2E_1" = "10" and "L_1L_2" = "00"
10	0000	"E_2E_1" = "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	0100	"E_2E_1" ≠ "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	Y001	Except the Foregoing
00	0000	"E_4E_3" ≠ "10", "E_2E_1" = "10" and "L_1L_2" ≠ "01"
00	0001	"E_4E_3" ≠ "10", "E_2E_1" = "10" and "L_1L_2" = "01"
00	0000	"E_2E_1" = "10"
00	0100	Except the Foregoing

8TH TABLE

Table (4) of Conversion Algorithm of Novel Encoding System

Original Data	Converted Code	Conditions
11	Y000	
01	0000	"E_6E_5" ≠ "10", "E_4E_3" = "10" and "E_2E_1" = "00"
01	0010	Except the Foregoing
10	0100	"E_2E_1" ≠ "10" and "L_1L_2" = "00"
10	0001	"E_2E_1" = "10" and "L_1L_2" = "00"
10	0000	"E_2E_1" = "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	0100	"E_2E_1" ≠ "10", "L_1L_2" = "10" and "L_3L_4" = "00"
10	Y001	Except the Foregoing
00	0000	"E_4E_3" ≠ "10", "E_2E_1" = "10" and "L_1L_2" ≠ "01"
00	0001	"E_4E_3" ≠ "10", "E_2E_1" = "10" and "L_1L_2" = "01"
00	0010	"E_4E_3" = "10" and "E_2E_1" = 10
00	0100	Except the Foregoing

Also in the case the Seventh Table is used as patterns when the conversion gives d and k, original data

··· 01 00 11 ··· results in converted codes

↓ ↓ ↓

·· "0010" "0100" "1000" ·· and d=2 holds. Also original data

... 01 10 00 00 ... results in converted codes

.. "0010" "0100" "0000" "0100" .. and k = 7 holds.

It is understood that d = 2 and k = 7 are given in this way and satisfy the Second Table.

Then regarding the conversion algorithm shown in the Seventh Table the ruling property of its conversion is considered. The Eighth Table is a conversion into which the Seventh Table has been partly revised and basically the same as the Seventh Table.

From the fundamental conversion table of the abovementioned Fifth Table it is understood that d = 2 and k = 7 are satisfied in the conversions except for the pattern ("10" "00") of the original data to be converted. Therefore upon the occurrence of the pattern ("10" "00"), d = 2 and k = 7 are caused to be satisfied in all the conversions of the patterns by changing the fundamental conversion table of the Fifth Table to the revised conversion methods as shown in the Seventh and Eighth Tables.

Fig. 3 is a block diagram of another embodiment to which another encoding system according to the present invention is applied and the timing chart of Fig. 4 is also used with that embodiment. Differences between the other embodiment shown in Fig. 3 and the one embodiment shown in Fig. 2 reside in that (a) a shift register (6A) has, in addition to the output terminals (Q_7 to Q_0), output terminals (Q_9 to Q_8), (b), an OR gate (30), a NOT gate (31) and an AND gate (32) newly added thereto (As a result, the output terminal Q_0 is directly connected to one input to

the AND gate (32), the output terminal (Q_1) is connected to the other input to the AND gate (32) through the NOT gate (31), an output terminal of the AND gate (32) is connected to an input terminal (A_0) to an ROM (7A), each of the output terminals (Q_2 to Q_7) is individually connected to each of the input terminals (A_1 to A_6), the output terminal (Q_8) is connected to one input to the OR gate (30), the output terminal (Q_9) is connected to the other input terminal to the OR gate (3) and an output terminal of the OR gate (30) is connected to the input terminal (A_7)), (c) the signal a shown in Fig. 4(a) is obtained at the output terminal (Q_4), and (d) the ROM (7A) has an alogrithm as shown in the following Ninth Table.

9TH RABLE

Table (2) of Algorithm of Converting ROM of Novel Encoding System

No.	Input Address								Output Pattern				Conditions for Input Address
	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_0	D_1	D_2	D_3	
1		1	1	1	1				1	0	0	0	
2		0	0	1	1				1	0	0	0	
3		0	1	1	1				0	0	0	0	
4		1	0	1	1				0	0	0	0	
5				0	1				0	0	1	0	
6		1	0	1	0	0	0		0	1	0	0	Except Address "A_1A_2" = "10"
7		1	0	1	0	0	0		0	0	0	1	
8		1	0	1	0	1	0	0	0	0	0	0	
9		1	0	1	0	1	0	0	0	1	0	0	Except Address "A_1A_2" = "10"
10		1	1	1	0				1	0	0	1	Except Addresses shown by Nos. 6 to 9
11		0	0	1	0				1	0	0	1	Ditto
12		0	1	1	0				0	0	0	1	Ditto
13		1	0	1	0				0	0	0	1	Ditto
14	0	1	0	0	0	0	1		0	0	0	0	Except Address "A_5A_6" = "01"
15	0	1	0	0	0	0	1		0	0	0	1	
16	1	1	0	0	0				0	0	0	0	
17				0	0				0	1	0	0	Except Addresses shown by Nos. 14 to 16
18	The Foregoing Excepted								0	0	0	0	

where $A_0 = Q_0 \times \bar{Q}_1$, $A_1 = Q_2$, $A_2 = Q_3$, $A_3 = Q_4$, $A_4 = Q_5$,

$A_5 = Q_6$, $A_6 = Q_7$ and $A_7 = Q_8 + Q_9$ hold

Portions with diagonal have any logics

It will be understood through that operation, that the pattern (11010001) of the original data shown in Fig. 4(a) is converted to a code pattern (10000010011000010) shown in Fig. 4(e) as in the embodiment of Fig. 2.

Then Fig. 5 shows a block diagram of one embodiment to which a decoding system according to the present invention is applied and Fig. 6 shows a timing chart for explaining the operation thereof. First a converted code sequence (Fig. 4(e)) is entered into an input terminal (10) and a clock signal g (Fig. 6(g)) synchronized therewith is entered into an input terminal (11). Then as during the encoding, the clock signal g is frequency divided into a signal i with a frequency divided by 2 (Fig. 6(i)) and a signal j with a frequency divided by 4 (Fig. 6(j)) by 1/2 frequency dividers (17) and (18) respectively. Also the entered converted code sequence is delayed one bit at a time within a shift register (parallel in-serial out)(13) with the clock signal g applied to a terminal (T) and delivered through the output terminals (Q_{12} to Q_0). (Assuming that Q_0 designates that output terminal through which a signal largest in delay is delivered, the delay is rendered small in the order of Q_1, Q_{12}.) It is now assumed that a signal A shown in Fig. 4(f) is being delivered to the output terminal (Q_6). On the other hand, signals at the output terminals (Q_0 to Q_3) are made into the logical sum by a logical sum (OR) gate (15) after which it is entered into an input terminal (A_0) to an ROM (SN 74S471 of TI firm or the like) Also the signals at the output terminals (Q_4 to Q_9) are entered into the

input terminals (A_1 to A_6) while the signals at the output terminals (Q_{10} to Q_{12}) are made into the logical sum by a logic sum (OR) gate (14). Thereafter it entered into the input terminal (A_7). The ROM (16) has a decoding conversion algorithm shown in the undermentioned Tenth or Eleventh Tables:

10TH RABLE

Table (1) of Decoding Algorithm of Converting ROM of Novel Encoding System

Input Address								Output Pattern	
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_0	D_1
			1	0	0	0		1	1
			0	0	1	0		0	1
			0	0	0	0	0	1	0
			0	1	0	0	0	1	0
				0	0	1		1	0
	1	0	0	0	0	0	1	1	1
1	0	1	0	0	0	0	1	1	1
Addresses Except for the Foregoing								0	0

The decoding algorithm of the Tenth Table is used upon decoding the code sequence converted by the embodiment of Fig. 2 and has an algorithm by which a decoding 4-bit codes (specified by the addresses A_3 to A_6) for the converted code sequence are decoded into the original 2-bit data in accordance with the conditions for a preceding and a succeeding code pattern (specified by the addresses A_0, A_1, A_2 and A_7). A decoded pattern is delivered to output

terminals (D_0 and D_1). This decoding algorithm of the converting ROM changes the output pattern through an algorithm of a preceeding and a succeeding pattern (specified by the address A_0, A_1, A_2, or A_7) only for two specified types of address patterns "A_3 to A_6" = "0000" and = "0100" among the 4-bit codes to be converted (specified by the addresses A_3 to A_6). A decoded output signal is entered into a shift register (parallel in-serial out)(19) at presetting terminals (G to H). On the other hand, the 1/2 frequency dividers (17) and (18) are put in synchronization with each other with a synchronizing signal h (entered into an input terminal (12) and shown in Fig. 6(h)) and generate a signal i with a frequency divided by 2 (Fig. 6(i)) and a signal j with a frequency divided by 4 (Fig. 6(j)) respectively. The shift register (19) latches presetting input signals thereto that is, signals at input terminals (H and G) with the timing signal j applied to its terminal (SF/L) and also delivers to an output terminal (2) data k (Fig. 6(k)) decoded with the demodulating clock signal i applied to its terminal (T) The decoding clock signal i is delivered to a clock output terminal (20). By viewing this status in the timing chart of Fig. 6, it will be understood that a pattern (1000001001000010) of the entered converted code sequence (=f) is decoded as decoded data k (11010001).

11TH RABLE

Table (2) of Decoding Algorithm of Converting ROM of Novel Encoding System

Input Address								Output Pattern	
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_0	D_1
			1	0	0	0		1	1
1	0	1	0	0	0	0	1	1	1
	1	0	0	0	0	0	1	1	1
			0	0	1	0		0	1
			0	1	0	0	0	1	0
1	0	0	0	0	0	1	0	1	0
	0	1	0	0	0	0	0	1	0
			1	0	0	1		1	0
	0	1	0	0	0	1		1	0
	1	0	0	0	0	1		1	0
The Foregoing Excepted								0	0

The decoding algorithm of the Eleventh Table is used in decoding the code seqpence converted by the embodiment of Fig. 3 and has an algorithm by which decoding 4-bit codes (specified by the addresses A_3 to A_6) are decoded into the original 2-bit data in accordance with the conditions for a preceeding and a succeeding code pattern (specified by the addresses A_0, A_1, A_2 and A_7). A decoded pattern is delivered to the output terminals (D_0 and D_1). This decoding algorithm of the converting ROM changes the output patterns through an algorithm of a preceeding and a succeeding pattern (specified by the address A_0, A_1, A_2 or A_7) only for three

specified types of the address patterns "A_3 to A_6" = "0000", = "0100" and "0001" among the 4-bit codes to be decoded (specified by the addresses A_3 to A_6). By viewing this status in the timing chart of Fig. 6, it will be understood that, as during the decoding by the embodiment of Fig. 2, a pattern (1000001001000010) of the entered decoded code sequence (=f) is decoded as decoded data k (11010001).

Further the Third and Fourth Tables for the encoding algorithms used for the purpose of describing the present invention are one concrete example of the present invention and the Seventh and Eighth Tables are other concrete examples of the present invention. Still another encoding algorithm may be used. That is, it is evident that in the encoding system, first, combinations of the original data patterns with the converted codes in the Third and Fourth Tables as well as in the Seventh and Eighth Tables are possible to be any combination of four types of patterns formed of two bits as four types of patterns shown by the original data. Also the logical algorithm and conditions of the converted codes reverse in order with respect to all the data. That is, for example, a converted code (Y001) is changed to (100Z) and $(E_2E_1) \rightarrow (L_1L_2)$, $(L_1L_2) \rightarrow (E_2E_1)$, $(L_3L_4) \rightarrow (E_4E_3)$ and $(E_4E_3) \rightarrow (L_3L_4)$ are effected. However Z at that time makes a complement logic of two bit immediately after the code bit Z in the converted code sequence. It is evident that the encoding system of the present invention may be formed of such an encoding method. Also even if the encoding patterns of the Third and Seventh Tables are partly revised and changed

as in the Fourth and Eighth Tables, there may be composed a similar encoding system having the ability to hold d = 2, k = 8 and k = 7 as predetermined.

INDUSTRIAL APPLICABILITY

As described above, the encoding and decoding systems of the present invention have the excellent ability, as a high density magnetic recording system, as compared with conventional other modulation systems such as in the Second Table, and a construction of the hardware is much simplified. Thus its practical merit is very large.

CLAIMS

1. A binary data encoding system characterized in that, upon dividing a binary data sequence at intervals of two bits and convetting said divided 2-bit data to codes each consisting of four bits, data are sensed within six bits preceding and continuous to said 2-bit data and also within six bits succeeding thereto, said data thus sensed are utilized to convert said 2-bit data to said 4-bit codes, and from not smaller than two to not greater than eight of code bits "0" are caused to exist between any code bit "1" of said converted code sequence and a code bit "1" next developed therein.

2. A binary data encoding system according to claim 1 characterized in that data are sensed within four bits preceding and continuous to the 2-bit data and also within four bits secceeding thereto.

3. A binary data encoding system according to claim 2 characterized in that data are sensed within two bits preceding and continuous to the 2-bit data and within four bits succeeding thereto and said 2-bit data are converted to the 4-bit data by using an algorithm of the following Conversion Table S1:

Conversion Table S1

Original Data	Converted Code	Conditions
A	Y000	
B	0010	
C	0100	"E_2E_1" ≠ "C" and "L_1L_2" = "D"
C	0001	"E_2E_1" = "C" and "L_1L_2" = "D"
C	0000	"E_2E_1" = "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	0100	"E_2E_1" ≠ "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	Y001	Except the Foregoing
D	0000	"E_2E_1" = "C"
D	0100	Except the Foregoing

where A to D : four types of patterns formed of 2-bit data and shown, for example, by A = "11", B = "01", C = "10" and D = "00"

Y : complement logic of logical sum of two bits immediately before code bit Y in converted code sequence

Y	Two Bits Immediately before Code Bit Y
1	"00"
0	Except for "00"

and

E_n : data bit preceding, by n-bits, 2-bit data to be converted in original data sequence

L_n : data bit succeeding, by n-bits, 2-bit data to be converted in original data sequence

4. A binary data encoding system according to claim 2 characterized in that data are sensed within four bits preceding and continuous to the 2-bit data and also within four bits succeeding thereto and said 2-bit data are converted to the 4-bit data by using an algorithm of the following Conversion Tables S2:

Conversion Table S2

Original Data	Converted Code	Conditions
A	Y000	
B	0010	
C	0100	"E_2E_1" ≠ "C" and "L_1L_2" = "D"
C	0001	"E_2E_1" = "C" and "L_1L_2" = "D"
C	0000	"E_2E_1" = "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	0100	"E_2E_1" ≠ "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	Y001	Except the Foregoing
D	0000	"E_2E_1" = "C" and "E_4E_3" ≠ "C"
D	0010	"E_2E_1" = "C" and "E_4E_3" = "C"
D	0100	Except the Foregoing

5. A binary data encoding system according to claim 2 characterized in that data are sensed within four bits preceding and continuous to the 2-bit data and also

within two bits succeeding thereto and said 2-bit data are converted to the 4-bit data by using an algorithm of the following Conversion Table S3.

Conversion Table S3

Original Data	Converted Code	Conditions
A	000Z	
B	0100	
C	0010	"E_2E_1" = "D" and "L_1L_2" ≠ "D"
C	1000	"E_2E_1" = "D" and "L_1L_2" = "C"
C	0000	"E_2E_1" = "C", "E_4E_3" = "D" and "L_1L_2" = "C"
C	0010	"E_2E_1" = "C", "E_4E_3" = "C" and "L_1L_2" ≠ "C"
C	100Z	Except the Foregoing
D	0000	"L_1L_2" = "C"
D	0010	Except the Foregoing

where A to D : four types of patterns formed of 2-bit data and shown, for example, by A = "11", B = "01", C = "10" and D = "00"

Z : complement logic of logical sum of two bits immediately after code bit "Z" in converted sequence

Y	Two Bits Immediately before Code Bit Y
1	"00"
0	Except for "00"

and

E_n : data bit preceding, by n-bits, 2-bit data to be converted in original data sequence

L_n : data bit succeeding, by n-bits, 2-bit data to be converted in original data sequence

6. A binary data encoding system according to claim 2 characterized in that data are sensed within four bits preceding and continuous to the 2-bit data and also within four bits succeeding thereto and said 2-bit data are converted to the 4-bit data by using an algorithm of the following Conversion Table S4:

Conversion Table S4

Original Data	Converted Code	Conditions
A	000Z	
B	0100	
C	0010	"E_2E_1" = "D" and "L_1L_2" ≠ "C"
C	1000	"E_2E_1" = "D" and "L_1L_2" = "C"
C	0000	"E_2E_1" = "C", "E_4E_3" = "D" and "L_1L_2" = "C"
C	0010	"E_2E_1" = "C", "E_4E_3" = "D" and "L_1L_2" ≠ "C"
C	100Z	Except the Foregoing
D	0000	"L_1L_2" = "C" and "L_3L_4" ≠ "C"
D	0100	"L_1L_2" = "C" and "L_3L_4" = "C"
D	0010	Except the Foregoing

7. A binary data encoding system according to claim 1 characterized in that from not smaller than two to not greater than seven of code bits "0" are caused to exist between any code bit "1" in the converted code sequence and a code bit "1" next developed therein.

8. A binary data encoding system according to claim 7 characterized in that data are sensed within four bits preceding and continuous to the 2-bit data and also within four bits succeeding thereto and said 2-bit data are converted to the 4-bit data by using an algorithm of the following Conversion Table S5:

Conversion Table S5

Original Data	Converted Code	Conditions
A	Y000	
B	0010	
C	0100	"E_2E_1" ≠ "C" and "L_1L_2" = "D"
C	0001	"E_2E_1" = "C" and "L_1L_2" = "D"
C	0000	"E_2E_1" = "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	0100	"E_2E_1" ≠ "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	Y001	Except the Foregoing
D	0000	"E_4E_3" ≠ "C", "E_2E_1" = "C" and "L_1L_2" ≠ "B"
D	0001	"E_4E_3" ≠ "C", "E_2E_1" = "C" and "L_1L_2" = "B"
D	0000	"E_4E_3" = "C" and "E_2E_1" = "C"
D	0100	Except the Foregoing

where A to D: four types of patterns, formed of 2-bit data and shown, for example, by A = "11", B = "01", C = "10" and D = "00"

Y : complement logic of ligical sum of two bits immediately before code bit Y in converted code sequence

Y	Two Bits Immediately before Code Bit Y
1	"00"
0	Except for "00"

and

E_n : data bit preceding, by n-bits, 2-bit data to be converted in original data sequence

L_n : data bit succeeding, by n-bits, 2-bit data to be converted in original data sequence

9. A binary data encoding system according to claim 7 characterized in that data are sensed within six bits preceding and continuous to the 2-bit data and also within four bits succeeding thereto and said 2-bit data are converted to the 4-bit data by using an algorithm of the following Conversion Table S6:

Conversion Table S6

Original Data	Converted Code	Conditions
A	Y000	
B	0000	"E_6E_5" ≠ "C", "E_4E_3" = "C" and "E_2E_1" = "D"
B	0010	Except the Foregoing
C	0100	"E_2E_1" ≠ "C" and "L_1L_2" = "D"
C	0001	"E_2E_1" = "C" and "L_1L_2" = "D"
C	0000	"E_2E_1" = "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	0100	"E_2E_1" ≠ "C", "L_1L_2" = "C" and "L_3L_4" = "D"
C	Y001	Except the Foregoing
D	0000	"E_4E_3" ≠ "C", "E_2E_1" = "C" and "L_1L_2" ≠ "B"
D	0001	"E_4E_3" ≠ "C", "E_2E_1" = "C" and "L_1L_2" = "B"
D	0010	"E_4E_3" = "C" and "E_2E_1" = "C"
D	0100	Except the Foregoing

10. A binary data encoding system according to claim 7 characterized in that data are sensed within four bits preceding and continuous to the 2-bit data and also within four bits succeeding thereto and said 2-bit data are converted to the 4-bit codes by using an algorithm of the following Conversion Table S7:

Conversion Table S7

Original Data	Converted Code	Conditions
A	000Z	
B	0100	
C	0010	"L_1L_2" ≠ "C" and "E_1E_2" = "D"
C	1000	"L_1L_2" = "C" and "E_2E_1" = "D"
C	0000	"L_1L_2" = "C", "E_2E_1" = "C" and "L_4L_3" = "D"
C	0010	"L_1L_2" ≠ "C", "E_2E_1" = "C" and "E_4E_3" = "D"
C	100Z	Except the Foregoing
D	0000	"L_3L_4" ≠ "C", "L_1L_2" = "C" and "E_2E_1" ≠ "B"
D	1000	"L_4L_3" ≠ "C", "L_1L_2" = "C" and "L_1L_2" = "B"
D	0000	"L_3L_4" = "C" and "L_1L_2" = "C"
D	0010	Except the Foregoing

where A to D : four types of patterns, formed of 2-bit data and shown, for example, by A = "11", B = "01", C = "10" and D = "00"

Y : complement logic of ligical sum of two bits immediately after code bit "Z" in converted code sequence

Z	Two Bits Immediately after Code Bit Y
1	"00"
0	Except for "00"

and

E_n : data bit preceding, by n-bits, 2-bit data to be converted in original data sequence

L_n : data bit succeeding, by n-bits, 2-bit data to be converted in original data sequence

11. A binary data encoding system according to claim 7 characterized in that data re sensed within four bits preceding and continuous to the 2-bit data and also within six bits succeeding thereto and said 2-bit data are converted to the 4-bit codes by using an algorithm of the following Conversion Table S8:

Conversion Table S8

Original Data	Converted Code	Conditions
A	000Z	
B	0000	"L_5L_6" ≠ "C", "L_3L_4" = "C" and "L_1L_2" = "D"
B	0100	Except the Foregoing
C	0010	"L_1L_2" ≠ "C" and "E_2E_1" = "D"
C	1000	"L_1L_2" = "C" and "E_2E_1" = "D"
C	0000	"L_1L_2" = "C", "E_2E_1" = "C" and "E_4E_3" = "D"
C	0010	"L_1L_2" ≠ "C", "E_2E_1" = "C" and "E_4E_3" = "D"
C	100Z	Except the Foregoing
D	0000	"L_3L_4" ≠ "C", "L_1L_2" = "C" and "E_2E_1" ≠ "B"
D	1000	"L_3L_4" ≠ "C", "L_1L_2" = "C" and "E_2E_1" = "B"
D	0100	"L_3L_4" = "C" and "L_1L_2" = "C"
D	0010	Except the Foregoing

12. A binary data decoding system characterized in that, upon dividing the code sequence converted in accordance with the binary data encoding system according to any of claims 2 to 6, at intervals of four bits, and decoding and converting said divided 4-bits codes into data codes each formed of two bits and when code patterns formed of said 4-bit codes have two specified types of the

code pattern, a preceding and a succeeding code pattern continuous to said 4-bit codes are sensed and said sensed code patterns are utilized to change a decoding algorithm for decoding said 4-bit data into said 2-bit data codes.

13. A binary data decoding system characterized in that, upon dividing the code sequence converted in accordance with the binary data encoding system according to any of claims 7 to 11 at intervals of four bits and decoding and converting said divided 4-bit codes into data codes each formed of two bits, and when code patterns formed of said 4-bit codes have three specified types of the code pattern, a preceding and a succeeding code pattern continuous to said 4-bit code are sensed, and said sensed code patterns are utilized to change a decoding algorithm for decoding said bit codes into said 2-bit data codes.

FIG. 1

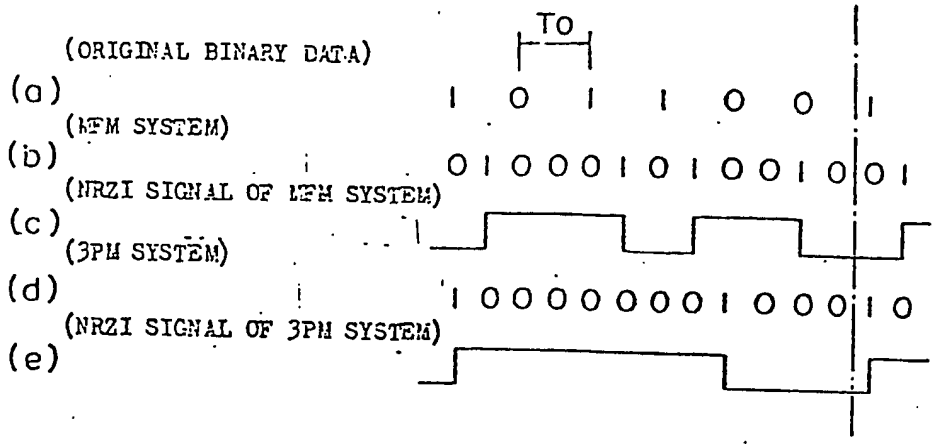


FIG. 2

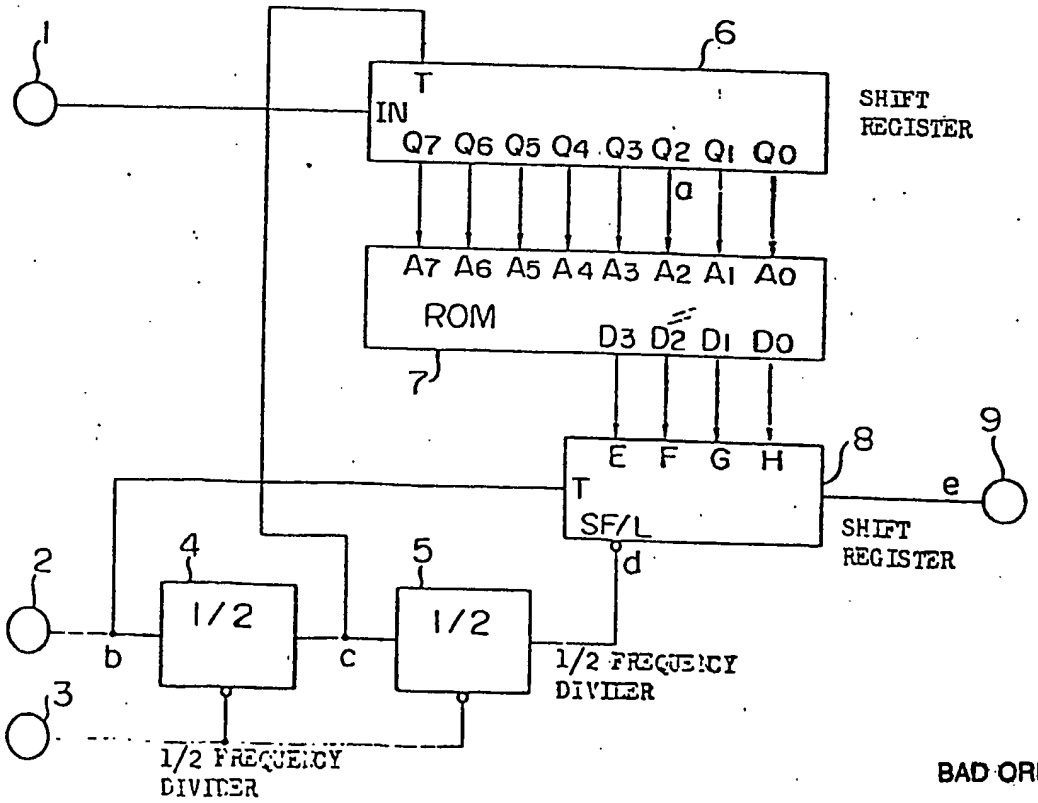


FIG. 3

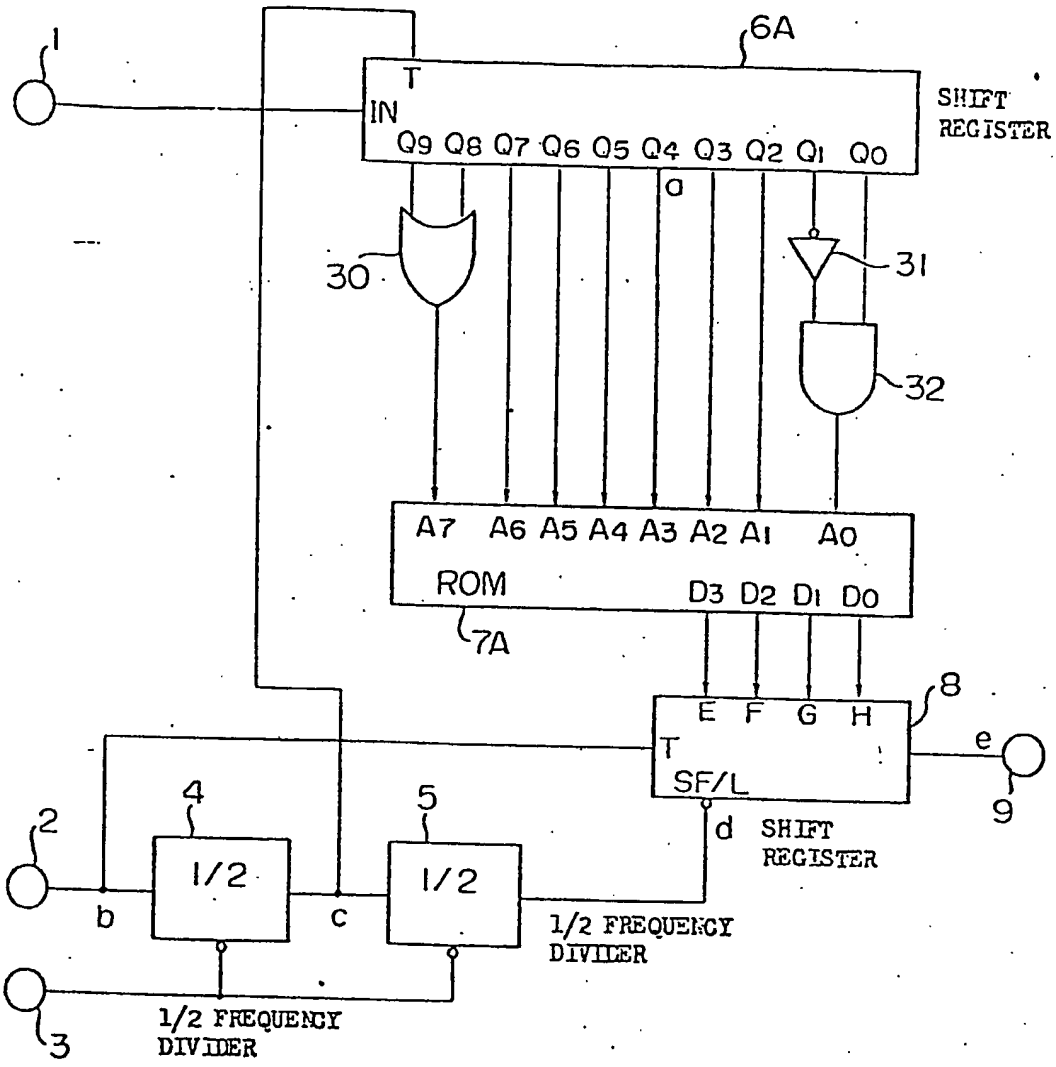

1
6A
T
IN
Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
SHIFT REGISTER
a
30
31
32
A7 A6 A5 A4 A3 A2 A1 A0
ROM
D3 D2 D1 D0
7A
8
E F G H
T
SF/L
e
9
d
SHIFT REGISTER
2
4
5
1/2
1/2
b
c
1/2 FREQUENCY DIVIDER
3
1/2 FREQUENCY DIVIDER

FIG. 4

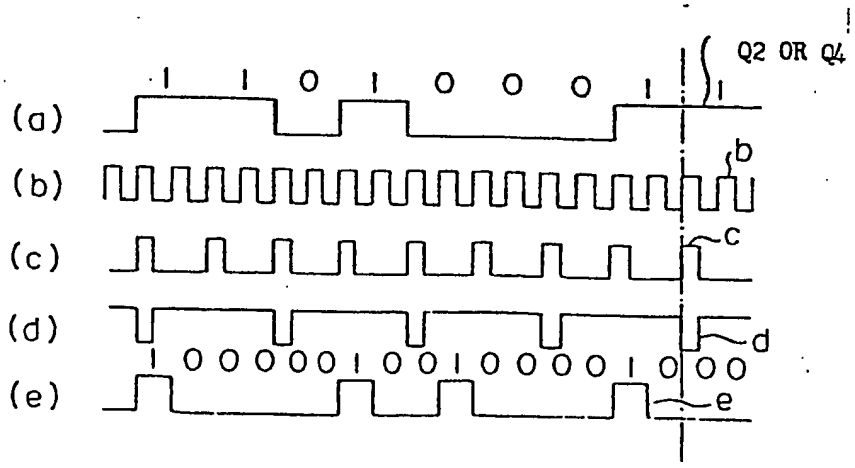

Q2 OR Q4
1 1 0 1 0 0 0 1 1
(a)
b
(b)
c
(c)
(d)
d
1 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0
(e)
e

FIG. 5

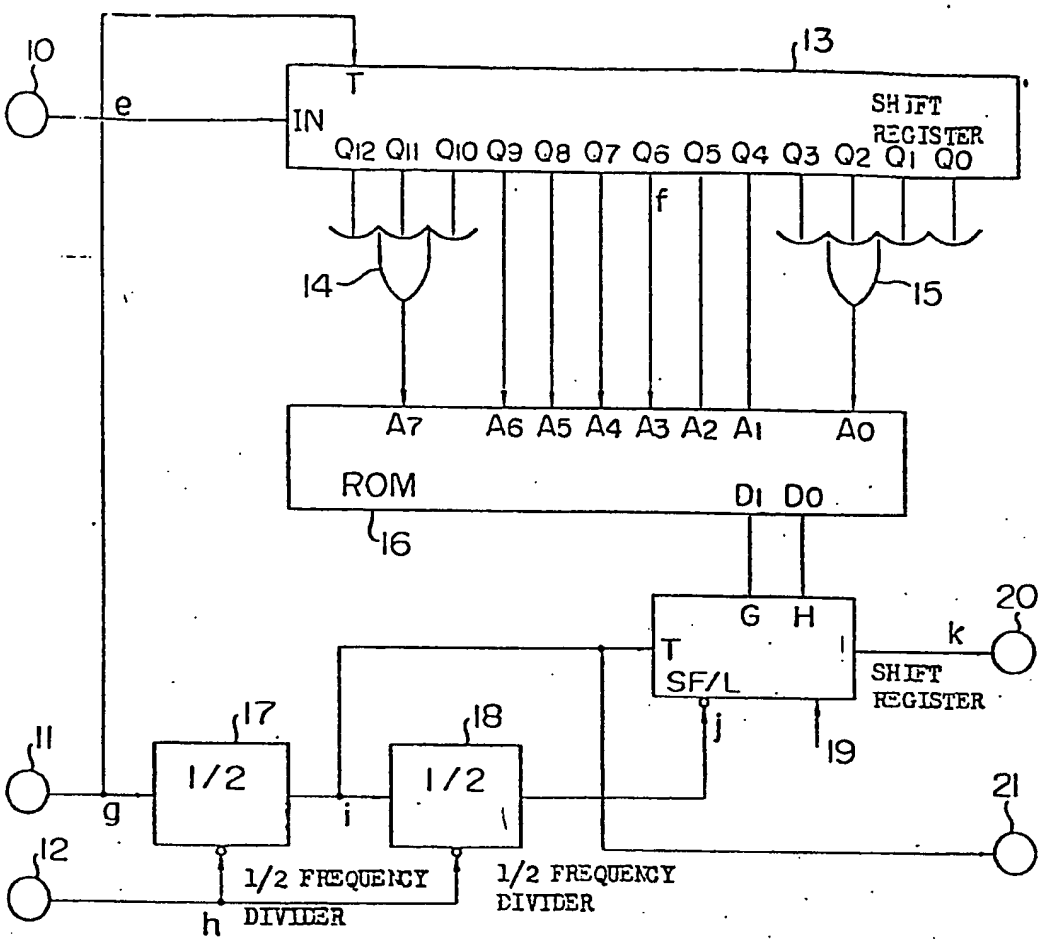
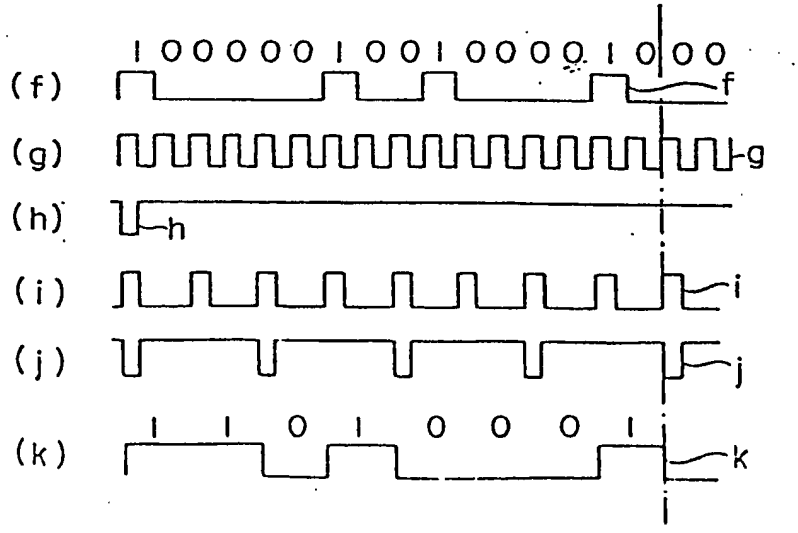

10
13
e
T
IN
SHIFT
REGISTER
Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
f
14
15
A7 A6 A5 A4 A3 A2 A1 A0
ROM
D1 D0
16
G H
20
k
T
SF/L
SHIFT
REGISTER
j
19
11
17
18
1/2
1/2
g
i
21
12
1/2 FREQUENCY
DIVIDER
1/2 FREQUENCY
DIVIDER
h

FIG. 6


1 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0
(f)
f
(g)
g
(h)
h
(i)
i
(j)
j
(k)
1 1 0 1 0 0 0 1
k

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP81/00218 00059224

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[3] G11B 5/09, H04L 25/49

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
I P C	G11B 5/09, H04L 25/49

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

Jitsuyo Shinan Koho 1968 - 1981

Kokai Jitsuyo Shinan Koho 1971 - 1981

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	IBM-Journal of Research and Development, Vol. 14, No. 4, (1970), P.A. Franaszek "Sequence-state Methods for Run-length -limited Coding", P. 376-383, Especially see Table 2 on P. 378 - 379	(1 - 13)
A	See JP, A, 53-11011 (Sperry Rand Corporation) December, 1978 (01.02.1978) Column 40, line 7 to Column 56, line 16, Figs. 6-10.	(1 - 13)

* Special categories of cited documents: [15]

"A" document defining the general state of the art

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [1]	Date of Mailing of this International Search Report [2]
November 30, 1981 (30.11.81)	December 14, 1981 (14.12.81)
International Searching Authority [1]	Signature of Authorized Officer [20]
Japanese Patent Office	